We claim:

1. A semiconductor apparatus, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a first region of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying a second region of said substrate surface;

a first region of said layer of semiconductor, overlying said layer of first material and having a first conductivity;

a second region of said layer of semiconductor, overlying said second region of said substrate surface and having a second conductivity; and

said first conductivity being substantially different from said second conductivity.

2. The semiconductor apparatus of claim 1, further comprising a layer of a second material overlying said second region of said substrate surface, said second region of said layer of semiconductor overlying said layer of said second material.

3. The semiconductor apparatus of claim 1, in which said first material is a polymer.

4. The semiconductor apparatus of claim 1, in which said first conductivity is at least about 100 times as large as said second conductivity.

5. The semiconductor apparatus of claim 1, in which said layer of semiconductor comprises crystal grains, and in which the average crystal grain size within said first region of said layer of semiconductor is at least about 10 times as large as the average crystal grain size within said second region of said layer of semiconductor.

6. The semiconductor apparatus of claim 1, in which said layer of semiconductor comprises crystal grains, and in which the average separation between crystal grains within said second region of said layer of semiconductor is at least about 10 times as large as the average separation between crystal grains within said first region of said layer of semiconductor.

7. The semiconductor apparatus of claim 1, in which said semiconductor is selected from the group consisting of: acenes, thiophenes, bithiophenes, phthalocyanines, naphthalene-1,4,5,8-tetracarboxylic diimide compounds, naphthalene-1,4,5,8-tetracarboxylic dianhydride, and 11,11,12,12-tetracyanonaphtho-2,6-quinodimethane.

8. The semiconductor apparatus of claim 1, further comprising:

a first gate electrode;

a first source electrode; and

a first drain electrode;

said first source and drain electrodes being in spaced apart conductive contact with a first channel portion of either said first or said second region of said layer of semiconductor, said first gate electrode being positioned to control a conductivity of said first channel portion.

9. The semiconductor apparatus of claim 2, in which said layer of first material overlies said second region of said substrate surface.

10. The semiconductor apparatus of claim 2, in which said second material is a polymer.

11. The semiconductor apparatus of claim 3, in which said first material is selected from the group consisting of: poly(para-vinyl phenol), poly(4-vinylpyridine), poly(2-vinylnaphthalene), poly(meta-vinyl phenol), poly(ortho-vinyl phenol), poly(para-vinyl phenol)-co-2-hydroxyethylmethacrylate, poly(2-vinylpyridine), poly(2-vinylnaphthalene-co-2-ethylhexyl acrylate, poly(1-vinylnaphthalene), and blends.

12. The semiconductor apparatus of claim 8, further comprising:

a second gate electrode;

a second source electrode; and

a second drain electrode;

said second source and second drain electrodes being in spaced apart conductive contact with a second channel portion of either said first region or said second region of said layer of semiconductor, said second gate electrode being positioned to control a conductivity of said second channel portion;

wherein said first and second channel portions are mutually isolated by an interposed region of said layer of semiconductor having a substantially lower conductivity than said conductivity of said first and second channel portions.

13. The semiconductor apparatus of claim 10, in which said second material is selected from the group consisting of: poly(n-butyl methacrylate), poly(vinylidene difluoride-co-methyl vinyl ether), polystyrene, poly(p-methoxystyrene), poly(vinylidene difluoride), poly(vinyl acetate), poly(vinyl propionate), poly(methoxy acetate), poly(n-propyl methacrylate), poly(isopropyl methacrylate), poly(n-pentyl methacrylate), poly(vinylidene difluoride-co-ethyl vinyl ether), poly(vinylidene difluoride-co-propyl vinyl ether), poly(dimethylaminoethyl methacrylate), poly(dimethylaminopropyl methacrylate), poly(aminopropyl methacrylate), poly(diethylaminoethyl methacrylate), and blends.

14. The semiconductor apparatus of claim 10, in which said second material comprises charge carrier traps.

15. The semiconductor apparatus of claim 11, in which said first material comprises poly(4-vinylpyridine).

16. The semiconductor apparatus of claim 11, in which said first material comprises poly(2-vinylnaphthalene).

17. The semiconductor apparatus of claim 13, in which said second material comprises poly(butyl methacrylate).

18. The semiconductor apparatus of claim 13, in which said second material comprises poly(vinylidine fluoride-co-methyl vinyl ether).

19. A method of making a semiconductor apparatus, comprising the steps of:

providing a substrate having a substrate surface;

providing a layer of a first material overlying a first region of said substrate surface; and

providing a layer of a semiconductor overlying said layer of first material and overlying a second region of said substrate surface;

a first region of said layer of semiconductor, overlying said layer of first material and having a first conductivity;

a second region of said layer of semiconductor, overlying said second region of said substrate surface and having a second conductivity; and

said first conductivity being substantially different from said second conductivity.

20. The method of claim 19, further comprising the step of:

providing a layer of a second material overlying said second region of said substrate surface, said second region of said layer of semiconductor overlying said layer of said second material.

21. The method of claim 20, in which said layer of first material overlies said second region of said substrate surface.

22. The method of claim 19, in which said first material is selected from the group consisting of: poly(para-vinyl phenol), poly(4-vinylpyridine), poly(2-vinylnaphthalene), poly(meta-vinyl phenol), poly(ortho-vinyl phenol), poly(para-vinyl phenol)-co-2-hydroxyethylmethacrylate, poly(2-vinylpyridine), poly(2-vinylnaphthalene-co-2-ethylhexyl acrylate, poly(1-vinylnaphthalene), and blends.

23. The method of claim 20, in which said second material is selected from the group consisting of: poly(n-butyl methacrylate), poly(vinylidene difluoride-co-methyl vinyl ether), polystyrene, poly(p-methoxystyrene), poly(vinylidene difluoride), poly(vinyl acetate), poly(vinyl propionate), poly(methoxy acetate), poly(n-propyl methacrylate), poly(isopropyl methacrylate),

poly(n-pentyl methacrylate), poly(vinylidene difluoride-co-ethyl vinyl ether), poly(vinylidene difluoride-co-propyl vinyl ether), poly(dimethylaminoethyl methacrylate), poly(dimethylaminopropyl methacrylate), poly(aminopropyl methacrylate), poly(diethylaminoethyl methacrylate), and blends.

24. An integrated circuit, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a plurality of first regions of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying a second region of said substrate surface;

a plurality of first regions of said layer of semiconductor, overlying said layer of first material and having a first conductivity;

a second region of said layer of semiconductor, overlying said second region of said substrate surface and having a second conductivity;

first and second gate electrodes;

first and second source electrodes;

first and second drain electrodes;

said first conductivity being substantially different from said second conductivity;

said first and second source and drain electrodes respectively being in spaced apart conductive contact with first and second channel portions of either said first regions or said second region of said layer of semiconductor, said first and second channel portions having respective first and second channel conductivities, said first and second gate electrodes being positioned to respectively control said first and second channel conductivities;

wherein said first and second channel portions are mutually isolated by an interposed region of said layer of semiconductor having a substantially lower conductivity than said first and second channel conductivities.

25. The integrated circuit of claim 24, further comprising a layer of a second material overlying said second region of said substrate surface, said second region of said layer of semiconductor overlying said layer of said second material.

26. A method of making an integrated circuit, comprising the steps of:

providing a substrate having a substrate surface;

providing a layer of a first material overlying a plurality of first regions of said substrate surface;

providing a layer of a semiconductor overlying said layer of first material and overlying a second region of said substrate surface;

providing a plurality of first regions of said layer of semiconductor, overlying said layer of first material and having a first conductivity;

providing a second region of said layer of semiconductor, overlying said second region of said substrate surface and having a second conductivity;

providing first and second gate electrodes;

providing first and second source electrodes;

providing first and second drain electrodes;

said first conductivity being substantially different from said second conductivity;

said first and second source and drain electrodes respectively being in spaced apart conductive contact with first and second channel portions of either said first regions or said second region of said layer of semiconductor, said first and second channel portions having respective first and second channel conductivities, said first and second gate electrodes being positioned to respectively control said first and second channel conductivities;

wherein said first and second channel portions are mutually isolated by an interposed region of said layer of semiconductor having a substantially lower conductivity than said first and second channel conductivities.